Zynq UltraScale+ MPSoC
Product Tables and Product Selection Guide

ZYNQ UltraSCALE+

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Zynq® UltraScale+™ MPSoCs

	CG Devices	EG Devices	EV Devices
Application Processor	**Dual**-core Arm® Cortex®-A53 MPCore™ up to **1.3GHz**	**Quad**-core Arm Cortex-A53 MPCore up to **1.5GHz**	**Quad**-core Arm Cortex-A53 MPCore up to **1.5GHz**
Real-Time Processor	Dual-core Arm Cortex-R5F MPCore up to **533MHz**	Dual-core ARM Cortex-R5 MPCore up to **600MHz**	Dual-core ARM Cortex-R5 MPCore up to **600MHz**
Graphics Processor		Mali™-400 MP2	Mali™-400 MP2
Video Codec			H.264 / H.265
Programmable Logic	81K–600K System Logic Cells	81K–1143K System Logic Cells	192K–504K System Logic Cells
Applications	• Sensor Processing & Fusion • Motor Control • Low-cost Ultrasound • Traffic Engineering	• Flight Navigation • Missile & Munitions • Military Construction • Secure Solutions • Networking • Cloud Computing Security • Data Center • Machine Vision • Medical Endoscopy	• Situational Awareness • Surveillance/Reconnaissance • Smart Vision • Image Manipulation • Graphic Overlay • Human Machine Interface • Automotive ADAS • Video Processing • Interactive Display

Zynq® UltraScale+™ MPSoCs: CG Devices

	Device Name[1]	ZU1CG	ZU2CG	ZU3CG	ZU3TCG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Processing System (PS)	Application Processor Unit – Processor Core	**Dual-core** Arm® Cortex®-A53 MPCore™ up to 1.3GHz								
	Application Processor Unit – Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB								
	Real-Time Processor Unit – Processor Core	**Dual-core** Arm Cortex-R5F MPCore up to 533MHz								
	Real-Time Processor Unit – Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core								
	External Memory – Dynamic Memory Interface	x16: DDR4 w/o ECC; x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC								
	External Memory – Static Memory Interfaces	NAND, 2x Quad-SPI								
	Connectivity – High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet								
	Connectivity – General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO								
	Integrated Block Functionality – Power Management	Full / Low / PL / Battery Power Domains								
	Integrated Block Functionality – Security	RSA, AES, and SHA								
	Integrated Block Functionality – AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor								
PS to PL Interface		12 x 32/64/128b AXI Ports								
Programmable Logic (PL)	Programmable Functionality – System Logic Cells (K)	81	103	154	157	192	256	469	504	600
	Programmable Functionality – CLB Flip-Flops (K)	74	94	141	144	176	234	429	461	548
	Programmable Functionality – CLB LUTs (K)	37	47	71	72	88	117	215	230	274
	Memory – Distributed RAM (Mb)	1.0	1.2	1.8	2.1	2.6	3.5	6.9	6.2	8.8
	Memory – Total Block RAM (Mb)	3.8	5.3	7.6	5.1	4.5	5.1	25.1	11.0	32.1
	Memory – UltraRAM (Mb)	-	-	-	14.0	13.5	18.0	-	27.0	-
	Clocking – Clock Management Tiles (CMTs)	3	3	3	1	4	4	4	8	4
	Integrated IP – DSP Slices	216	240	360	576	728	1,248	1,973	1,728	2,520
	Integrated IP – PCI Express®	-	-	-	1x Gen3x8	2x Gen3x8[2]	2x Gen3x8[2]	-	1x Gen3x16 & 1x Gen3x8	-
	Integrated IP – 150G Interlaken	-	-	-	-	-	-	-	-	-
	Integrated IP – 100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	-	-
	Integrated IP – AMS - System Monitor	2	2	2	2	2	2	2	2	2
	Transceivers – GTH Transceivers[3]	-	-	-	8	16	16	24	24	24
	Transceivers – GTY Transceivers	-	-	-	-	-	-	-	-	-
	Speed Grades – Extended[4]	-1 -2 -2L				-1 -2 -2L -3				
	Speed Grades – Industrial	-1 -1L -2								

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. ZU4 and ZU5 also support 1x Gen3x16 based on available GTH.
3. GTH data rates are package dependent:
   a) Maximum 12.5Gb/s in SFVC784 and SFVD784
   b) Maximum 16.3Gb/s in all other packages
4. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

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Zynq® UltraScale+™ MPSoCs: EG Devices

		Device Name[1]	ZU1EG	ZU2EG	ZU3EG	ZU3TEG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.5GHz												
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB												
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5F MPCore™ up to 600MHz												
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core												
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz												
		Memory	L2 Cache 64KB												
	External Memory	Dynamic Memory Interface	x16: DDR4 w/o ECC; x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC												
		Static Memory Interfaces	NAND, 2x Quad-SPI												
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet												
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO												
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains												
		Security	RSA, AES, and SHA												
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor												
PS to PL Interface			12 x 32/64/128b AXI Ports												
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	81	103	154	157	192	256	469	504	600	653	747	926	1,143
		CLB Flip-Flops (K)	74	94	141	144	176	234	429	461	548	597	682	847	1,045
		CLB LUTs (K)	37	47	71	72	88	117	215	230	274	299	341	423	523
	Memory	Max. Distributed RAM (Mb)	1.0	1.2	1.8	2.1	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
		Total Block RAM (Mb)	3.8	5.3	7.6	5.1	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
		UltraRAM (Mb)	-	-	-	14.0	13.5	18.0	-	27.0	-	22.5	31.5	28.7	36.0
	Clocking	Clock Management Tiles (CMTs)	3	3	3	1	4	4	4	8	4	8	4	11	11
	Integrated IP	DSP Slices	216	240	360	576	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
		PCI Express®	-	-	-	1x Gen3x8	2x Gen3x8[2]	2x Gen3x8[2]	-	1x Gen3x16 & 1x Gen3x8[3]	-	2x Gen3x16 & 2x Gen3x8[3]	-	3x Gen3x16 & 1x Gen3x8[3]	3x Gen3x16 & 2x Gen3x8[3]
		150G Interlaken	-	-	-	-	-	-	-	-	-	1	-	2	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	-	-	2	-	2	4
		AMS - System Monitor	1	1	1	2	1	1	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	-	8	16	16	24	24	24	32	24	44	44
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-	-	-	16	-	28	28
	Speed Grades	Extended[4]	-1 -2 -2L				-1 -2 -2L -3					-1 -2 -2L -3			
		Industrial	-1 -1L -2												

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. ZU4 and ZU5 also support 1x Gen3x16 based on available GTH.
3. PCIe block configuration dependent on available transceivers.
4. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

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Zynq® UltraScale+™ MPSoCs: EV Devices

		Device Name[1]	ZU4EV	ZU5EV	ZU7EV
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.5GHz		
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB		
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5F MPCore™ up to 600MHz		
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core		
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz		
		Memory	L2 Cache 64KB		
	External Memory	Dynamic Memory Interface	x16: DDR4 w/o ECC; x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC		
		Static Memory Interfaces	NAND, 2x Quad-SPI		
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet		
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains		
		Security	RSA, AES, and SHA		
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor		
PS to PL Interface			12 x 32/64/128b AXI Ports		
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	192	256	504
		CLB Flip-Flops (K)	176	234	461
		CLB LUTs (K)	88	117	230
	Memory	Max. Distributed RAM (Mb)	2.6	3.5	6.2
		Total Block RAM (Mb)	4.5	5.1	11.0
		UltraRAM (Mb)	13.5	18.0	27.0
	Clocking	Clock Management Tiles (CMTs)	4	4	8
	Integrated IP	DSP Slices	728	1,248	1,728
		Video Codec Unit (VCU)	1	1	1
		PCI Express® Gen 3x16	2x Gen3x8[2]	2x Gen3x8[2]	1x Gen3x16 & 1x Gen3x8[3]
		150G Interlaken	-	-	-
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-
		AMS - System Monitor	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	16	16	24
		GTY 32.75Gb/s Transceivers	-	-	-
	Speed Grades	Extended[4]	-1 -2 -2L -3		
		Industrial	-1 -1L -2		

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2.ZU4 and ZU5 also support 1x Gen3x16 based on available GTH.
3.PCIe block configuration dependent on available transceivers.
4.-2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

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Zynq® UltraScale+™ MPSoCs

PS I/Os(1), 3.3V High-Density (HD) I/O, 1.8V High-Performance (HP) I/Os

PS-GTR 6Gb/s, GTH 16.3Gb/s, GTY 32.75Gb/s

Pkg Footprint(2,3)	Dimensions (mm)	Ball Pitch (mm)	ZU1	ZU2	ZU3	ZU3T	ZU4	ZU5	ZU6	ZU7	ZU9	ZU11	ZU15	ZU17	ZU19
A484	19x19	0.8	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0										
A494	9.5x15	0.5	170, 24, 58 4, 0, 0												
A530	9.5x16	0.5		170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0										
A625	21x21	0.8	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0										
C784(4)	23x23	0.8	214, 24, 156, 4, 0, 0	214, 96, 156 4, 0, 0	214, 96, 156 4, 0, 0	214, 72, 52 4, 4, 0	214, 96, 156 4, 4, 0	214, 96, 156 4, 4, 0							
D784(4)	23x23	0.8				214, 72, 52 4, 8, 0									
B900	31x31	1.0					214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0					
C900	31x31	1.0							214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		
B1156	35x35	1.0							214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		
C1156	35x35	1.0								214, 48, 312 4, 20, 0		214, 48, 312 4, 20, 0			
B1517	40x40	1.0										214, 72, 416 4, 16, 0		214, 72, 572 4, 16, 0	214, 72, 572 4, 16, 0
F1517	40x40	1.0								214, 48, 416 4, 24, 0		214, 48, 416 4, 32, 0			
C1760	42.5x42.5	1.0										214, 96, 416 4, 32, 16		214, 96, 416 4, 32, 16	214, 96, 416 4, 32, 16
D1760	42.5x42.5	1.0												214, 48, 260 4, 44, 28	214, 48, 260 4, 44, 28
E1924	45x45	1.0												214, 96, 572 4, 44, 0	214, 96, 572 4, 44, 0

Notes:
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale devices with the same sequence.
3. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*..
4. GTH transceivers in the C784 and D784 packages support data rates up to 12.5Gb/s.

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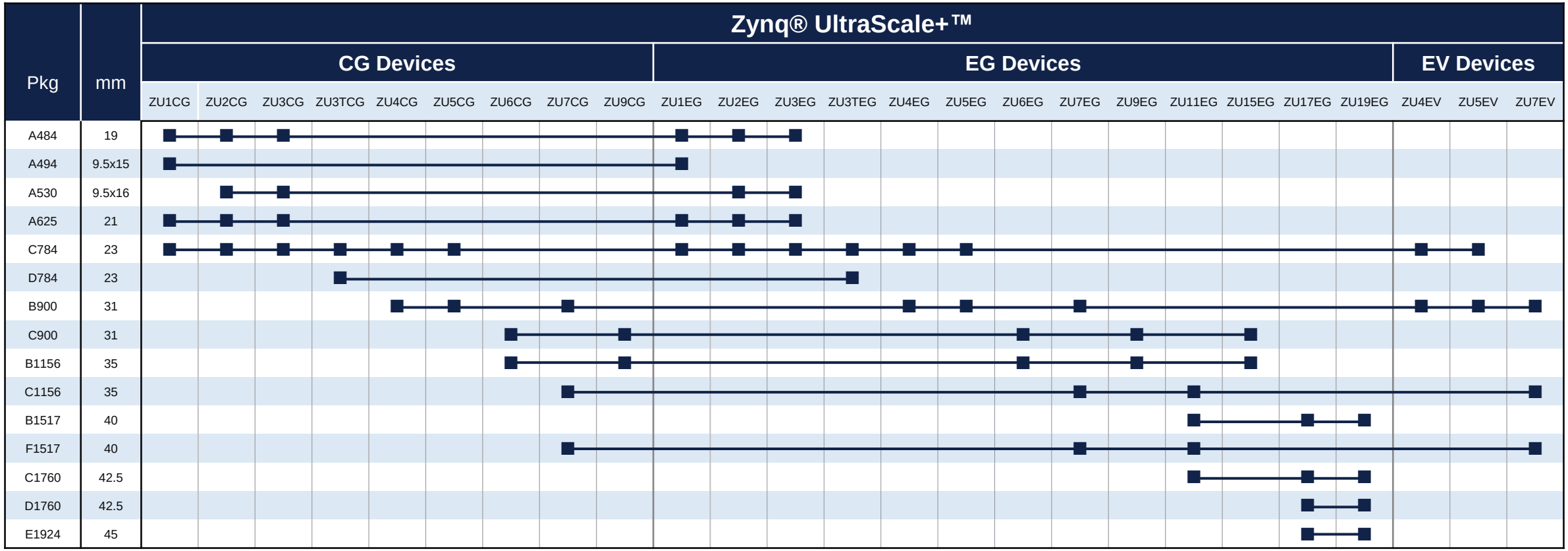
Zynq® UltraScale+™ MPSoC Device Migration Table

The Zynq UltraScale+ family provides footprint compatibility to enable users to migrate designs from one device to another. Any two packages with the same footprint identifier code (last letter and number sequence) are footprint compatible.



Zynq® UltraScale+™ MPSoC Ordering Information

Device Name					Device Attributes				Footprint		
XC	ZU	#	E	G	-1	F	F	V	A	#	E
Commercial Grade	Zynq UltraScale +	Value Index*	Processor System Identifier C: Dual APU Dual RPU E: Quad APU Dual RPU Single GPU	Engine Type G: General Purpose V: Video	Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power -3: Fastest	F: Flip-chip w/ 1.0mm Ball Pitch S: Flip-chip w/ 0.8mm Ball Pitch U: InFO w/ 0.5mm Ball Pitch	F: Lid B: Lidless	V: RoHS 6/6	Package Designator	Package Pin Count	Temperature Grade (E, I)

E = Extended (Tj = 0°C to +100°C)
I = Industrial (Tj = –40°C to +100°C)

Note: -L2E (Tj = 0°C to +110°C). Refer to DS891, *Zynq UltraScale+ MPSoC Overview for additional information.*

**T in ZU3T value index denotes increase in resources and transceivers vs. ZU3.*

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